

REMARKS

The disclosure has been objected to as referring, at page 10, line 9, to a patent which is not clearly identified. In the above Amendment to the Specification, this error has been corrected; the patent being referred to is 5,638,121, which is discussed and incorporated by reference elsewhere in the Specification.

The Drawings, in particular Figures 5, 6, and 3, have been objected to. Attached hereto are proposed "Replacement Sheets" which show changes to the Drawings as mandated in the Office Action.

The Examiner has indicated allowable subject matter in claims 6-9 and 17-18 as filed. In the above Amendment, Independent Claim 1 has been amended to include the limitations of claim 6 as filed, as well as intermediate claim 5. The limitation of claim 7 has been added to establish an antecedent basis in claim 1 as amended. Other claims have been amended to clarify dependence from Claim 1 as amended. Similarly, Independent Claim 11 has been amended to include the limitations of claim 17 as filed, as well as intermediate claim 15. Other claims have been amended to clarify dependence from Claim 11 as amended.

The claims are therefore in condition for allowance.

No additional fee is believed to be required for this amendment; however, the undersigned Xerox Corporation attorney authorizes the charging of any necessary fees, other than the issue fee, to Xerox Corporation Deposit Account No. 24-0025.

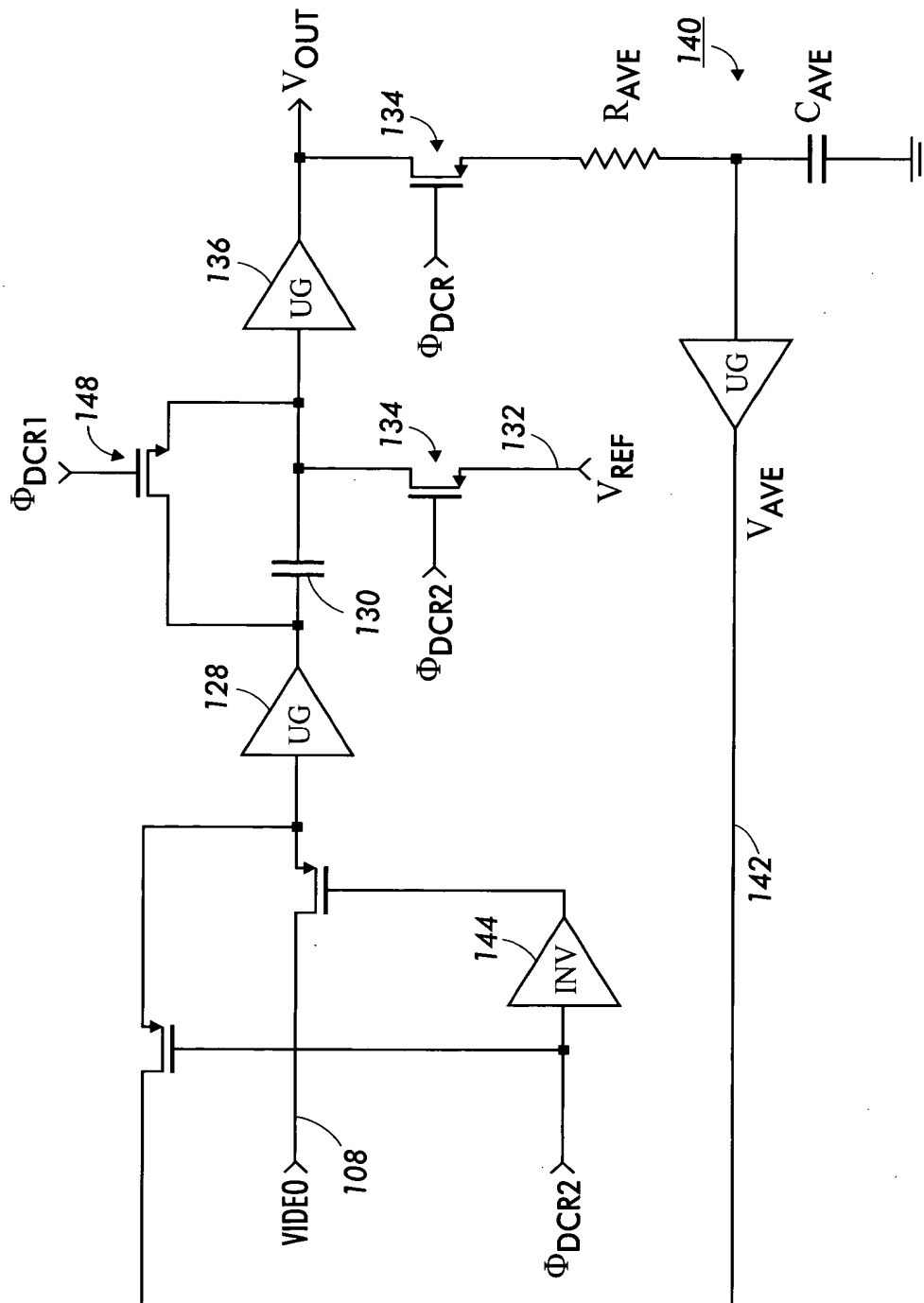
In the event the Examiner considers personal contact advantageous to the disposition of this case, he is hereby requested to call the undersigned attorney at (585) 423-3811, Rochester, NY.

Respectfully submitted,

A handwritten signature in cursive script, reading "Robert Hutter", written in dark ink. The signature is fluid and stylized, with a horizontal line drawn beneath the name.

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July 14, 2004
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**FIG. 3**
PRIOR ART

The diagram illustrates a video signal processing circuit. At the bottom, a horizontal line represents the **VIDEO** input. Four pixel signals, Φ_{PIXEL1} , Φ_{PIXEL2} , Φ_{PIXEL3} , and Φ_{PIXEL4} , are shown as inputs to a series of four comparators (labeled 200). Each comparator also receives a reference signal Φ_{RP1} through Φ_{RP4} and a common clock signal Φ_{S} . The outputs of these comparators are connected to a feedback loop. The feedback loop includes a resistor R_{AVE} and a capacitor C_{AVE} connected to ground. The output of the feedback loop is connected to a summing junction (labeled 140) and a buffer (labeled UG). The output of the buffer is connected to the V_{REF} input of the comparators. The output of the summing junction is connected to the output of the video signal processing circuit, labeled V_{OUT} . The circuit also includes a feedback capacitor C_{MUX} and a feedback resistor R_{MUX} connected to ground. The output of the feedback loop is also connected to a buffer (labeled UG) and a resistor R_{AVE} connected to ground. The output of the feedback loop is connected to the output of the video signal processing circuit, labeled V_{OUT} .

